In the Claims

Please amend claims 1-46 as follows:

1. (original) Apparatus for providing port priority functions in a very long instruction word (VLIW) processor comprising:

a register of at least double word width having at least two single word write enables; and

means for resolving a write priority conflict between instructions on a single word basis thereby enabling operation to complete normally on a single word portion of said register of at least double word width that is not in conflict even though at least one other single word portion of said register of at least double word width is in conflict.

2. (original) The apparatus of claim 1 wherein said register of at least double word width has a width of at least 64-bits, the single word is a 32-bit word, a double word is a 64-bit word, and port priorities are defined on the 32-bit word basis to control said write enable signals to a register file containing said register of at least double word width.

3. (original) The apparatus of claim 2 wherein double word and single word data type instructions are mixed within a common very long instruction word (VLIW).

4. (original) The apparatus of claim 1 further comprising port priority logic to control the at least two single word write enables.

5. (original) The apparatus of claim 1 wherein a plurality of said at least double word width registers are contained in a register file which is a compute register file (CRF), an address register file (ARF) or any register file in the processor complex wherein multiple instructions may conflict on subdata types of operations.

6. (original) The apparatus of claim 1 wherein non-conflicting word operations are completed normally while conflicting word operations are prioritized for completion utilizing the port priority logic.

7. (original) The apparatus of claim 6 wherein the port priority logic further comprises:

a plurality of write selection multiplexers for selectably writing a single word to a selected location in said register subject to priority controlled load enable and multiplexer selection signals.

8. (original) The apparatus of claim 7 further comprising:

a plurality of write port address decoders producing output location select signals; and

a plurality of logical OR gates connected to the write port address decoders' output location select signals and producing the priority controlled load enable signals as their outputs.

9. (original) The apparatus of claim 8 further comprising:

a plurality of priority encoders also connected to the write port address decoders' output location select signals to produce write selection multiplexer select signals.

10. (original) The apparatus of claim 5 wherein the port priority logic establishes port priority from highest priority to lowest priority order as follows: memory load ALU, MAU, and DSU operations.

11. (original) The apparatus of claim 1 wherein said means for resolving a write priority conflict comprises port priority logic that is programmable.

12. (original) The apparatus of claim 11 further comprising a load very long instruction word (LVa) instruction employing three priority bits to specify up to eight port

priority orderings for a very long instruction word (VLIW) being loaded into VLIW instruction memory (VIM).

13. (original) The apparatus of claim 12 wherein said three priority bits are loaded into VIM and when an execute VLIW (XV) instruction is executed, the port priority bits are read out of the VIM and the port priority logic is setup prior to the VLIW execution cycle.

14. (original) A method for providing port priority functions in a very long instruction word (VLIW) processor comprising:

establishing a register file having registers of at least double word width and having at least two single word write enables; and

resolving a write priority conflict between instructions on a single word basis thereby enabling operation to complete normally on a single word portion of one register of at least double word width that is not in conflict even though at least one other single word portion of said one register of at least double word width is in conflict.

15. (original) The method of claim 14 wherein said at least double word width is defined as 64-bits, the single word is defined as a 32-bit word, and port priorities are defined on the 32-bit word basis to control said write enable signals to a computer register file (CRF) containing the register file.

16. (original) The method of claim 15 further comprising the step of:

mixing double word and single word data type instructions within a common very long instruction word (VLIW).

17. (original) The method of claim 14 further comprising the step of:

utilizing port priority logic to control the at least two single word write enables.

18. (original) The method of claim 17 further comprising the step of:

completing non-conflicting word operations while conflicting word operations are prioritized for completion utilizing the port priority logic.

19. (original) The method of claim 14 further comprising the step of:

utilizing port priority logic that is programmable to resolve the write priority conflict.

20. (original) Apparatus for providing port priority functions in a very long instruction word (VLIW) processor comprising:

a register file having registers of at least single word width and having at least two half-word write enables; and

means for resolving a write priority conflict between instructions on a half-word basis thereby enabling operation to complete normally on a half-word portion of one register of at least single word width that is not in conflict even though at least one other half-word portion of the said one register of at least single word width is in conflict.

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